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		7735－4M		21/ 88	Ａ

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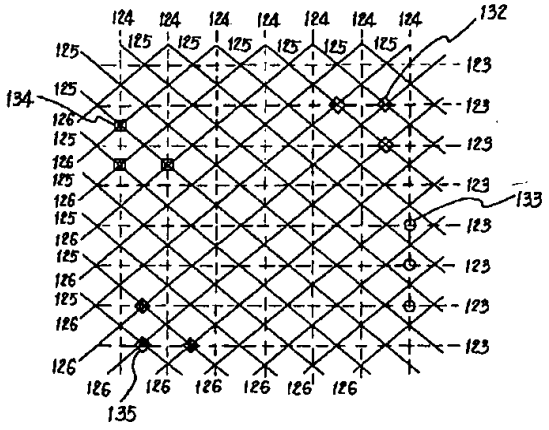
(54)【発明の名称】　半導体集積回路装置

(57)【要約】

【目的】半導体チップ内のハードマクロ間の配線領域を小さくし、チップ全体の面積を縮小する。

【構成】ハードマクロ上に設けた第３層配線１２３及び第４層配線１２４と、これらと斜めに交差する第５層配線１２５及び第６層配線１２６を配置し、第２層配線と第３層配線第３層配線１２３を接続する第２スルーホールと１３２と、第５層配線１２５と第６層配線１２６を接続する第５スルーホール１３５と、第４層配線１２４と第５層配線１２５を接続する第４スルーホール１３４と、第３層配線１２３と第４層配線１２４を接続する第３スルーホール１３３を設けることにより、ハードマクロ上を最短距離で配線可能にする。



123：第3層配線　124：第4層配線
125：第5層配線　126：第6層配線
132：第2スルーホール　133：第3スルーホール
134：第4スルーホール　135：第5スルーホール

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【特許請求の範囲】

【請求項1】　半導体チップ上に設けた第1層配線及び第2層配線を用いて基本トランジスタ素子間を接続して形成されたハードマクロと、前記ハードマクロの相互間を接続する横方向に配置した第3層配線と、前記第3層配線に対して垂直に交差して格子を形成する縦方向に配置した第4層配線と、前記第3層配線及び第4層配線の交点以外の第3層配線及び第4層配線に対してそれぞれ斜めに交差し且つ互いに交差する第5層配線及び第6層配線を備えたことを特徴とする半導体集積回路装置。

【請求項2】　第5層配線及び第6層配線がハードマクロ上に配置された請求項1記載の半導体集積回路装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体集積回路装置に関し、特にチップ内のハードマクロ間の配線に関する。

【0002】

【従来の技術】一般に半導体集積回路装置は、装置の小型化、システムの要求に合わせて年々集積度が高くなっている。

【0003】従来の半導体集積回路装置は、図4に示すように、図面上の横方向に配置した第1層配線221と、図面上の縦方向に配置した第2層配線222及び第1層配線221と同様に横方向に配置して配線ピッチを第1層配線221の2倍にした第3層配線223が配置され、第1層配線221及び第2層配線222で最小配線間隔の格子を構成し、格子点にて第1層配線221と第2層配線222を接続する第1スルーホール231と、第2層配線222及び第3層配線223で作られた格子に対し、格子点にて第2層配線222と第3層配線223を接続する第2スルーホール232を備えている。

【0004】図5及び図6は従来の半導体集積回路装置の第1及び第2の例を示すレイアウト図である。

【0005】図5及び図6に示すように、LSIチップ11上に形成したハードマクロAとハードマクロB間を第1層配線221及び第2層配線222を使用して構成する場合に、図4に示した配線ピッチに従って、ハードマクロAからハードマクロBへ配線接続を行なう場合、ハードマクロB上を第1層配線221及び第2層配線222のみを用いて配線する事ができないので、図5に示すように第3層配線223を用いてハードマクロB上を通過させる方法と、図6に示すようにハードマクロA，Bの周囲の配線領域13内に第1層配線221及び第2層配線222を用いて引き回す配線方法がある。図5に示す前者は、ハードマクロAの出力を第2層配線222を用いて引き出し、第2スルーホール232で第3層配線223に接続させ、ハードマクロB上を第3層配線223を用いて通過させ、通過後、第2スルーホール232で第2層配線222に接続させ、その後第1スルーホール231を用いて第1層配線221に接続させ、再度第1スルーホール231を用いて第2層配線222に接続させ、ハードマクロBの入力となる構成になっている。図6に示す後者は、ハードマクロAの上部出力を第2層配線222を用いて引き出し、第1スルーホール231を用いて第1層配線221に接続し、チップ左上まで配線し、第1スルーホール231を用いて第2層配線222に接続し、左下まで配線を延ばし、再度第1スルーホール231を用いて第1層配線221に接続し、再々度第1スルーホール231を用いて第2層配線222に接続し、ハードマクロBの入力となる構成になっている。

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【0006】

【発明が解決しようとする課題】従来の半導体集積回路装置では、図4に示すように図の横方向の第1層配線221，図の縦方向の第2層配線222及び第1層配線221と同様に図の横方向の第3層配線223と、第1層配線221と第2層配線222を接続する第1スルーホール231，第2層配線222と第3層配線223で作られた最小格子の交点に第2層配線222と第3層配線223を接続する第2スルーホール232を有して構成されており、ハードマクロ内の配線を第1層配線221及び第2層配線222用いて構成している為、ハードマクロ間配線は、ハードマクロ上を第1層配線221及び第2層配線222を用いて通過させる事ができず、ハードマクロ上を通過せずに空領域に配線を引き回したり、又は図の横方向のみに第3層配線223を用いてハードマクロ上を通過させ、その後空領域で第1層配線221及び第2層配線222に接続させて配線を行なっていた。そのため、最短に配線することができず、配線の引き回しを行わなければならず、配線領域は拡大し、チップ全体として面積が大きくなるという欠点があった。

【0007】本発明の目的は、多層配線を用いることにより配線領域を小さくし、さらにはチップ全体の面積を縮小することのできる半導体集積回路装置を提供する事にある。

【0008】

【課題を解決するための手段】本発明の半導体集積回路装置は、半導体集積回路上に設けた第1層配線と第2層配線を用いて基本トランジスタ素子間を接続して形成されたハードマクロと、ハードマクロの相互間を接続する横方向に配置した第3層配線と、第3層配線に対して垂直に交差して格子を形成する縦方向に配置した第4層配線と、第3層配線及び第4層配線の交点以外の第3層配線及び第4層配線に対してそれぞれ斜めに交差し且つ互いに交差する第5層配線及び第6層配線とを備えている。

【0009】

【実施例】次に、本発明について図面を参照して説明する。

【００１０】図１は本発明の一実施例を説明するためのレイアウト図である。

【００１１】図１に示すように、半導体チップ上に設けた第１層配線と第２層配線を用いて基本トランジスタ素子間を接続して形成されたハードマクロを互いに接続するための信号線用配線において、図面上の横方向に設置した第３層配線１２３と、第３層配線１２３に対して図面上の縦方向に配置した第４層配線１２４と、第３層配線１２３及び第４層配線１２４の交点を通らず、第３層配線１２３及び第４層配線１２４に対しそれぞれ斜めに交差し、かつ互いに交差する第５層配線１２５と、第６層配線１２６とを有して構成する。また、第３層配線１２３及び第４層配線１２４で作られた最小格子に対して、第４層配線１２４の半ピッチずれた点でハードマクロ内で用いられている第２層配線２２２と、ハードマクロ間配線に用いる第３層配線１２３を第２スルーホール１３２で接続し、第３層配線１２３及び第４層配線１２４で作られた最小格子の交点で、第３層配線１２３と、第４層配線１２４を第３スルーホール１３３で接続し、第３層配線１２３及び第４層配線１２４で作られた最小格子において、第３層配線１２３の半ピッチずれた点で、第４層配線１２４と、第５層配線１２５を第４スルーホール１３４で接続し、第２スルーホール１３２と同様に第３層配線１２３及び第４層配線１２４で作られた最小格子において第４層配線１２４の半ピッチずれた点で、第５層配線と第６層配線１２６を第５スルーホール１３５で接続する。

【００１２】図２は本発明の第１の応用例を示すレイアウト図である。

【００１３】図２に示すように図１に示した配線ピッチに従ってハードマクロＡの図面上に下部出力からハードマクロＢの図面上下部入力へ配線接続を行なう場合、ハードマクロＡ内の信号線用配線である第２層配線２２２出力をハードマクロ間配線へ接続する配線領域１３内の第２スルーホールを用いて第３層配線１２３に接続配線し第３スルーホール１３３を用いて第４層配線１２４へ接続配線し、ハードマクロＡ上の第４スルーホール１３４を用いて第５層配線１２５に接続し、ハードマクロＢの図面上右下まで配線し、配線領域１３上の第４スルーホール１３４を用いて第４層配線１２４に接続配線し、第３スルーホール１３３を用いて第３層配線１２３へ接続配線し、第２スルーホール１３２を用いてハードマクロＢ内の信号線用配線である第２層配線２２２入力に接続する。

【００１４】図３は本発明の第２の応用例を示すレイアウト図である。

【００１５】図３に示すように、ハードマクロＡの図面上上部出力からハードマクロＢの図面下部入力へ配線接続を行なう場合、ハードマクロＡ内の信号線用配線である第２層配線２２２出力をハードマクロ間配線へ接続する第２スルーホール１３２を用いて第３層配線１２３に接続配線し、第３スルーホール１３３を用いて第４層配線１２４に接続配線し、第４スルーホール１３４を用いて第５層配線１２５に接続配線し、第５スルーホール１３５を用いて第６層配線１２６に接続し、ハードマクロＢ左下まで配線し、第５スルーホール１３５を用いて第５層配線１２５に接続配線し、第４スルーホール１３４を用いて第４層配線１２４に接続配線し、第３スルーホール１３３を用いて第３層配線１２３に接続配線し、第２スルーホール１３２を用いてハードマクロＢ内の信号線用配線である第２層配線２２２入力に接続する。

【００１６】

【発明の効果】以上説明したように本発明は、半導体チップ上の第１層配線と第２層配線を用いて基本トランジスタ間を接続して形成されたハードマクロを互いに接続する場合、ハードマクロ上を横方向，縦方向，斜め方向に配線することができるので配線の引き回しがなくなり、また、第３層配線及び第４層配線で作られた最小格子に第２層配線と第３層配線を接続する第２スルーホールと、第３層配線と第４層配線を接続する第３スルーホールと、第４層配線と第５層配線を接続する第４スルーホールと、第５層配線と第６層配線を接続する第５スルーホールを配置するので、比較的短い距離で配線可能となる。本実施例によれば、ｘ座標，ｙ座標ともに異なる２つの端子を継ぐために従来２単位長必要であった配線長が$2^{1/2}$単位長で可能となるので、従来の技術と比べ面積として約５０％配線領域が小さくなり、また従来配線領域はチップ面積の６０％程度を占有していたため、チップ面積としては約３０％（＝６０％×０．５）の縮小を得ることが可能となる。

【００１７】このように、本発明では、配線領域を小さくし、さらにはチップ全体の縮小化を得ることができるという効果を有する。

【図面の簡単な説明】

【図１】本発明の一実施例を説明するためのレイアウト図。

【図２】本発明の第１の応用例を示すレイアウト図。

【図３】本発明の第２の応用例を示すレイアウト図。

【図４】従来の配線の配置を説明するためのレイアウト図。

【図５】従来の半導体集積回路装置の第１の例を示すレイアウト図。

【図６】従来の半導体集積回路装置の第２の例を示すレイアウト図。

【符号の説明】

１１　ＬＳＩチップ

１３　配線領域

１２３，２２３　第３層配線

１２４　第４層配線

１２５　第５層配線

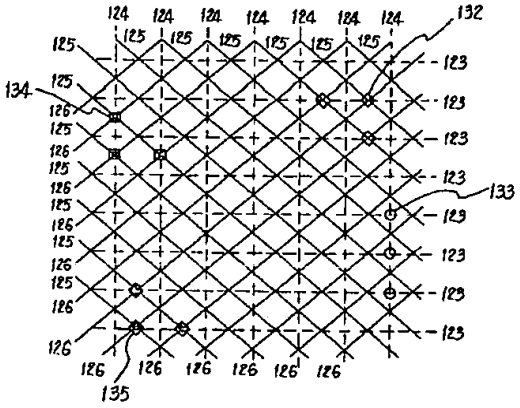
5

126　第6層配線
132，232　第2スルーホール
133　第3スルーホール
134　第4スルーホール
135　第5スルーホール

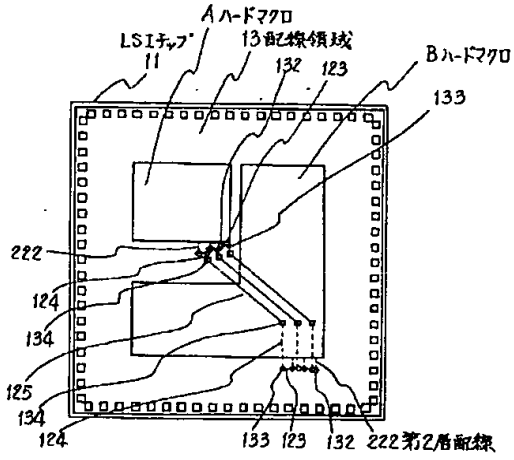
6

221　第1層配線
222　第2層配線
231　第1スルーホール
A，B　ハードマクロ

【図1】

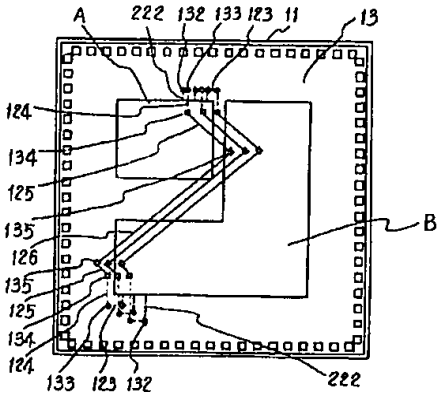


【図2】

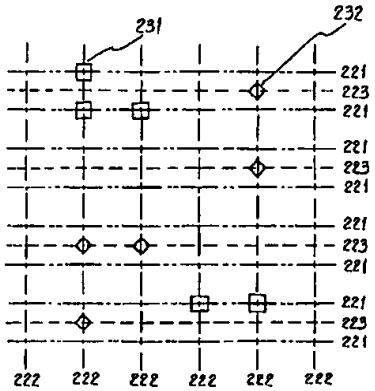


123：第3層配線　124：第4層配線
125：第5層配線　126：第6層配線
132：第2スルーホール　133：第3スルーホール
134：第4スルーホール　135：第5スルーホール

【図3】

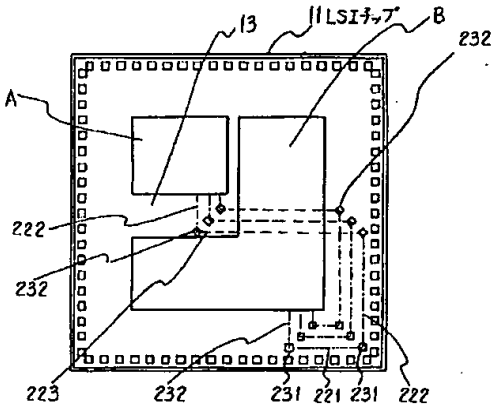


【図4】

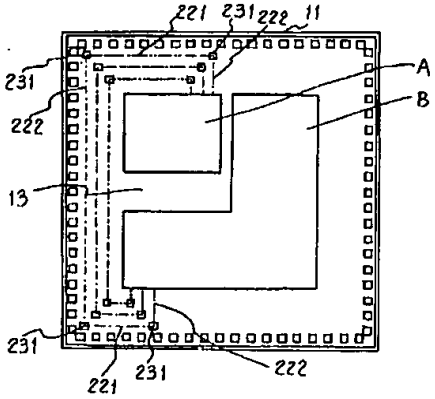


221：第1層配線　222：第2層配線
223：第3層配線　231：第1スルーホール
232：第2スルーホール

【図5】


13
LSIチップ
B
232
A
222
232
223
232
231
221
231
222

【図6】


221
231
222
11
231
A
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231
221
231
222

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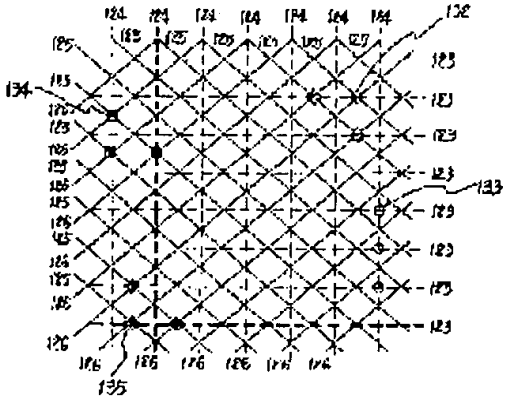
(22)Date of filing : **27.02.1992**

(71)Applicant : **NEC IC MICROCOMPUT SYST LTD**
(72)Inventor : **KUBOTA MASAKO**

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To reduce the area of a chip as a whole by a method wherein a wiring region on a hard macro inside a semiconductor chip is made small.
CONSTITUTION: The following are arranged: third-layer interconnections 123 and fourth-layer interconnections 124 which are formed on a hard macro; and fifth-layer interconnections 125 and sixth-layer interconnections 126 which cross them obliquely. In addition, the following are formed: second through holes 132 which connect second-layer interconnections to the thirdlayer interconnections 123; fifth through holes 135 which connect the fifth-layer interconnections 125 to the sixth-layer interconnections 126; fourth through holes 134 which connect the fourth-layer interconnections 124 to the fifth-layer interconnections 125; and third through holes 133 which connect the third-layer interconnections 123 to the fourth-layer interconnections 124. Thereby, a wiring operation can be performed at a shortest distance on the hard macro.



LEGAL STATUS

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[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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(54) **[Title of Invention]**

Semiconduct r Integrated Circuit Apparatus

(57) **[Abstract]**

[Purpose]

To diminish wiring areas between hard macros inside a semiconductor chip and thus reduce the overall chip area.

[Constitution]

A third layer of wiring 123 and fourth layer of wiring 124 provided on hard macros, and a fifth layer of wiring 125 and a sixth layer of wiring 126 intersecting diagonally therewith, are configured, and second through holes 132 connecting a second layer of wiring and the third layer of wiring 123, fifth through holes 135 connecting the fifth layer of wiring 125 and the sixth layer of wiring 126, fourth through holes 134 connecting the fourth layer of wiring 124 and the fifth layer of wiring 125, and third through holes 133 connecting the third layer of wiring 123 and the fourth layer of wiring 124 are provided, thereby making it possible to implement wiring across the shortest distances on the hard macros.

[Claims]

[Claim 1] A semiconductor integrated circuit apparatus comprising:

hard macros, formed by making connections between basic transistor elements using a first layer of wiring and a second layer of wiring provided on a semiconductor chip;

a third layer of wiring, configured in the horizontal direction, interconnecting between said hard macros;

a fourth layer of wiring, configured in the vertical direction, intersecting said third layer of wiring perpendicularly and forming a lattice; and

a fifth layer of wiring and sixth layer of wiring that, respectively, intersect diagonally said third layer of wiring and said fourth layer of wiring at points where said third layer of wiring and said fourth layer of wiring do not intersect, and that also intersect each other.

[Claim 2] The semiconductor integrated circuit apparatus according to Claim 1, wherein said fifth layer of wiring and said sixth layer of wiring are configured on [or above] the hard macros.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention concerns a semiconductor integrated circuit apparatus, and more particularly the wiring between hard macros in a chip.

[0002]

[Prior Art]

Year by year the degree of integration in semiconductor integrated circuit apparatuses in general rises higher as such apparatuses become smaller and as such higher integration is demanded by systems.

[0003]

In a conventional semiconductor integrated circuit apparatus, as diagrammed in Fig. 4, a first layer of wiring 221, placed in the horizontal direction in the diagram, a second layer of wiring 222 placed in the vertical direction in the diagram, and a third layer of wiring 223, placed in the horizontal direction as the first layer of wiring 221, the wiring pitch whereof is made twice that of the first layer of wiring 221, are provided, configuring a lattice having minimal wiring intervals with the first layer of wiring 221 and the second layer of wiring 222, and this apparatus further comprises first through holes 231 connecting the first layer of wiring 221 and the second

layer of wiring 222 at the lattice points, and second through holes 232 connecting the second layer of wiring 222 and the third layer of wiring 223 at the lattice points, for the lattice made by the second layer of wiring 222 and third layer of wiring 223.

[0004]

Fig. 5 and 6 are layout diagrams representing a first and a second example of a conventional semiconductor integrated circuit apparatus.

[0005]

When a hard macro A and hard macro B, formed on an LSI chip 11, as diagrammed in Fig. 5 and 6, are configured such that a first layer of wiring 221 and a second layer of wiring 222 are used therebetween, if wiring connections are made from the hard macro A to the hard macro B according to the wiring pitch indicated in Fig. 4, it is not possible to implement wiring on the hard macro B using only the first layer of wiring 221 and second layer of wiring 222. Wherefore, there are two methods, namely the method of using a third layer of wiring 223 to transit across the hard macro B, diagrammed in Fig. 5, and the method of implementing circuitous wiring, within the wiring area 13 about the periphery of the hard macros A and B, using the first layer of wiring 221 and second layer of wiring 222, diagrammed in Fig. 6. In the former method, diagrammed in Fig. 5, the output of the hard macro A is led out using the second layer of wiring 222, connected to the third layer of wiring 223 with a second through hole 232, and made to transit across the hard macro B using the third layer of wiring 223, whereupon, after transit, it is connected to the second layer of wiring 222 with a second through hole 232, connected subsequently to the first layer of wiring 221 using a first through hole 231, and connected to the second layer of wiring 222 using a first through hole 231 again, becoming the input to the hard macro B. In the latter method, diagrammed in Fig. 6, the upper output of the hard macro A is led out using the second layer of wiring 222, connected to the first layer of wiring 221 using a first through hole 231, wired as far as the upper left [corner] of the chip, connected to the second layer of wiring 222 using a first through hole 231, wired down as far as the lower left [corner], connected to the first layer of wiring 221 using a first through hole 231 again, and connected to the second layer of wiring 222 using a first through hole 231 again, becoming the input to the hard macro B.

[0006]

[Problems Which the Present Invention Attempts to Solve]

A conventional semiconductor integrated circuit apparatus, as diagrammed in Fig. 4, comprises a first layer of wiring 221 in the horizontal direction in the diagram, a second layer of wiring 222 in the vertical direction in the diagram, a third layer of wiring 223 in the same horizontal direction in the diagram as the first layer of wiring 221, first through holes 231 for connecting the first layer of wiring 221 and the second layer of wiring 222, and second through holes 232 for connecting the second layer of wiring 222 and the third layer of wiring 223 at the smallest lattice intersections made by the second layer of wiring 222 and third layer of wiring 223, and configures the wiring inside the hard macros using the first layer of wiring 221 and

second layer of wiring 222, wherefore, in wiring between the hard macros, the first layer of wiring 221 and second layer of wiring 222 cannot be made to transit across the hard macros, but the wiring must be routed around the open space, without transiting across a hard macro, or, alternatively, wiring must be effected wherein the hard macro is transited using the third layer of wiring 223 only in the horizontal direction of the diagram, and subsequently connected in the open area to the first layer of wiring 221 and second layer of wiring 222. For this reason, it is not possible to effect the shortest wiring, circuitous wiring is necessary, the wiring area expands, and the overall chip area becomes larger, all of which constitute problems.

[0007]

An object of the present invention is to provide a semiconductor integrated circuit apparatus wherein the wiring area is made smaller by employing multi-layer wiring, and the overall chip area can be reduced.

[0008]

[Means Used to Solve the Problems]

The semiconductor integrated circuit apparatus of the present invention comprises: hard macros, formed by making connections between basic transistor elements using a first layer of wiring and a second layer of wiring provided on a semiconductor integrated circuit; a third layer of wiring, configured in the horizontal direction, interconnecting between the hard macros; a fourth layer of wiring, configured in the vertical direction, intersecting the third layer of wiring perpendicularly and forming a lattice; and a fifth layer of wiring and sixth layer of wiring that, respectively, intersect diagonally the third layer of wiring and the fourth layer of wiring at points where the third layer of wiring and the fourth layer of wiring do not intersect, and that also intersect each other.

[0009]

[Embodiments]

The present invention is now described with reference to the drawings.

[0010]

Fig. 1 is a layout diagram for describing one embodiment of the present invention.

[0011]

In signal line wiring for interconnecting hard macros formed by interconnecting basic transistor elements using a first layer of wiring and a second layer of wiring provided on a semiconductor chip, as diagrammed in Fig. 1, the configuration comprises a third layer of wiring 123 placed in the horizontal direction on the diagram, a fourth layer of wiring 124 placed in the vertical direction on the diagram relative to the third layer of wiring 123, and a fifth layer of wiring 125 and sixth layer of wiring 126 that intersect diagonally with the third layer of wiring

123 and the fourth layer of wiring 124, respectively, without passing through the intersections between the third layer of wiring 123 and the fourth layer of wiring 124, and that also intersect each other. Also, a second layer of wiring 222 used inside the hard macros at points shifted by half a pitch on the fourth layer of wiring 124 relative to the smallest lattice made by the third layer of wiring 123 and fourth layer of wiring 124, and the third layer of wiring 123 used in interconnecting the hard macros are connected with second through holes 132, the third layer of wiring 123 and the fourth layer of wiring 124 are connected with third through holes 133 at the smallest lattice intersections made by the third layer of wiring 123 and the fourth layer of wiring 124, the fourth layer of wiring 124 and the fifth layer of wiring 125 are connected by fourth through holes 134 at points shifted by half a pitch on the third layer of fwiring 123 in the smallest lattice made by the third layer of wiring 123 and the fourth layer of wiring 124, and, similarly, the fifth layer of wiring [125] and sixth layer of wiring 126 are connected by fifth through holes 135 at points shifted by half a pitch on the fourth layer of wiring 124 in the smallest lattice made by the third layer of wiring 123 and the fourth layer of wiring 124.

[0012]

Fig. 2 is a layout diagram representing a first application example for the present invention.

[0013]

When, as diagrammed in Fig. 2, wiring connection is made from the lower output, on the diagram, of the hard macro A to the lower input, on the diagram, of the hard macro B, following the wiring pitch diagrammed in Fig. 1, the output of the second layer of wiring 222 that constitutes the signal line wiring inside the hard macro A is interconnected to the third layer of wiring 123 using the second through holes inside the wiring area 13 connecting to the wiring between the hard macros, interconnected to the fourth layer of wiring 124 using the third through holes 133, connected to the fifth layer of wiring 125 using the fourth through holes 134 on the hard macro A, effecting wiring as far as the lower right [corner] of the hard macro B in the diagram, interconnected to the fourth layer of wiring 124 using the fourth through holes 134 on the wiring area 13, interconnected to the third layer of wiring 123 using the third through holes 133, and connected to the input of the second layer of wiring 222 that constitutes the signal line wiring inside the hard macro B, using the second through holes 132.

[0014]

Fig. 3 is a layout diagram for a second application example of the present invention.

[0015]

When interconnecting from the upper output, in the diagram, of the hard macro A to the lower input, in the diagram, of the hard macro B, as diagrammed in Fig. 3, the output of the second layer of wiring 222 constituting the signal wiring inside the hard macro A is interconnected to the third layer of wiring 123 using the second through holes 132 which connect to the wiring between the hard macros, interconnected to the fourth layer of wiring 124 using the

third through holes 133, interconnected to the fifth layer of wiring 125 using the fourth through holes 134, connected to the sixth layer of wiring 126 using the fifth through holes 135, wiring as far as the lower left [corner] of the hard macro B, interconnected to the fifth layer of wiring 125 using the fifth through holes 135, interconnected to the fourth layer of wiring 124 using the fourth through holes 134, interconnected to the third layer of wiring 123 using the third through holes 133, and connected to the input of the second layer of wiring 222 that constitutes the signal line wiring inside the hard macro B, using the second through holes 132.

[0016]

[Merits of the Invention]

With the present invention, as described in the foregoing, when hard macros formed by interconnecting basic transistors using a first layer of wiring and a second layer of wiring on a semiconductor chip are mutually connected, it is possible to effect wiring on the hard macros in the horizontal, vertical, and diagonal directions, wherefore circuitous wiring is done away with. Furthermore, second through holes connecting the second layer of wiring and the third layer of wiring, third through holes connecting the third layer of wiring and the fourth layer of wiring, fourth through holes connecting the fourth layer of wiring and the fifth layer of wiring, and fifth through holes connecting the fifth layer of wiring and the sixth layer of wiring are provided in the smallest lattice made by the third layer of wiring and the fourth layer of wiring, so wiring can be done over comparatively short distances. With this embodiment, moreover, what previously required two unit lengths of wiring in order to connect two terminals having different x coordinates and y coordinates can be done with 2 1/2 unit lengths of wiring. Therefore, as compared to the prior art, the wiring area is reduced by approximately 50% in terms of surface area, and, because the wiring area previously occupied 60% or so of the chip area, the chip area can be reduced by approximately 30% (= 60% x 0.5).

[0017]

Thus the present invention is beneficial in that, by the use thereof, wiring areas can be made smaller, and overall chip size can be reduced.

[Brief Description of the Drawings]

Fig. 1 is a layout diagram for describing one embodiment of the present invention;

Fig. 2 is a layout diagram representing a first application example of the present invention;

Fig. 3 is a layout diagram representing a second application example of the present invention;

Fig. 4 is a layout diagram for describing the placement of conventional wiring;

Fig. 5 is a layout diagram representing a first example of a conventional semiconductor

integrated circuit apparatus; and

Fig. 6 is a layout diagram representing a second example of a conventional semiconductor integrated circuit apparatus.

[Explanation of Symbols]

11 LSI chip

13 Wiring area

123, 223 Third layer of wiring

124 Fourth layer of wiring

125 Fifth layer of wiring

126 Sixth layer of wiring

132, 232 Second through holes

133 Third through hole

134 Fourth through hole

135 Fifth through hole

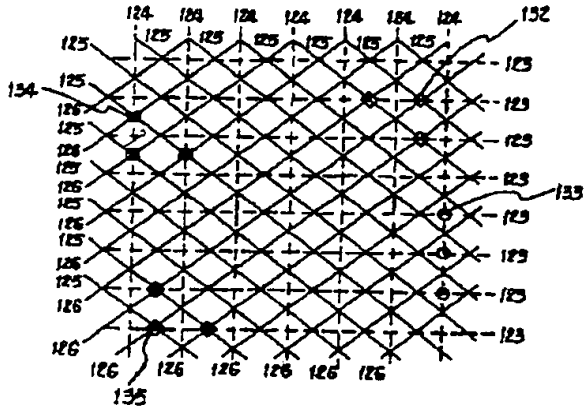
221 First layer of wiring

222 Second layer of wiring

231 First through hole

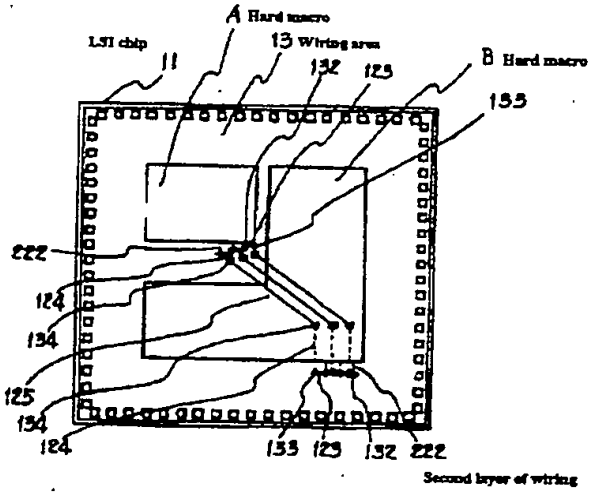
A, B Hard macros

[Figure 1]

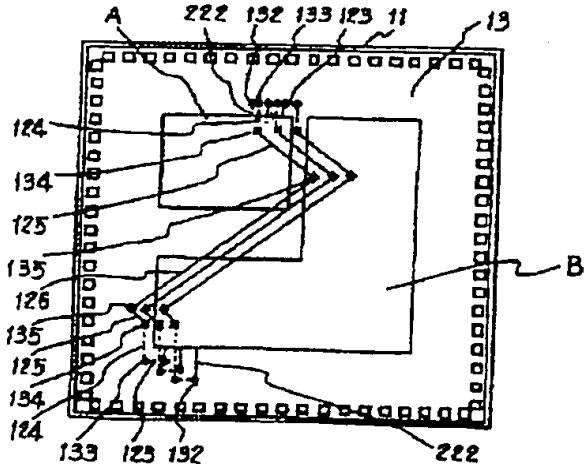


123 : Third layer of wiring
124 : Fourth layer of wiring
125 : Fifth layer of wiring
126 : Sixth layer of wiring
132 : Second through hole
133 : Third through hole
134 : Fourth through hole
135 : Fifth through hole

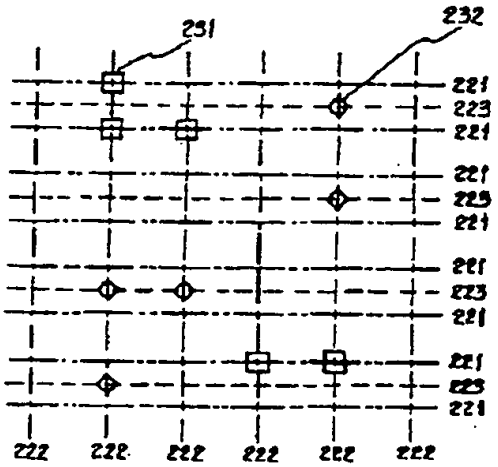
[Figure 2]



[Figure 3]

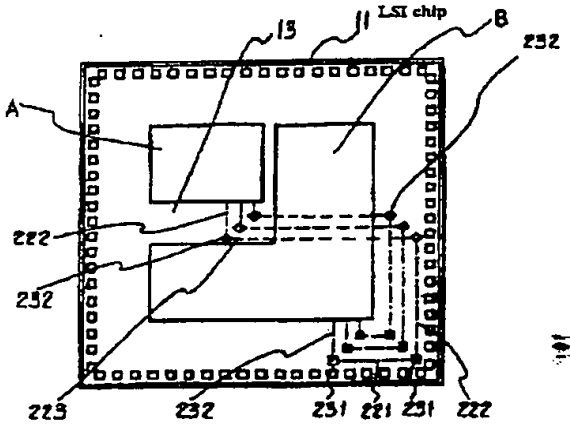


[Figure 4]



221 : First layer of wiring
222 : Second layer of wiring
223 : Third layer of wiring
231 : First through hole
232 : Second through hole

[Figure 5]



[Figure 6]